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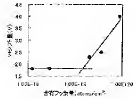
(54) MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE



(57)Abstract:

PROBLEM TO BE SOLVED: To provide a manufacturing method of an a-Si TFT having an excellent reliability, by improving the film quality of its semiconductor layer wherein fluorine has been so entrapped conventionally in its manufacturing process as to cause its on/off resistances to deteriorate, although an SiNx film and an a-Si film are formed continuously in it by a plasma CVD method as its gate insulation film and as its semiconductor layer and it has otherwise originally excellent on/off resistances.
SOLUTION: A TFT is so created that the fluorine content of its semiconductor layer created by a plasma CVD method has a small value not larger than 1.0× 1019 (atoms/cm3). By such improvement of the film quality of its semiconductor layer as to make good the film quality present near the interface between its gate insulation film and its semiconductor layer, there can be provided the a-Si TFT of an excellent characteristic having a small shifting quantity of its Vt which is caused by its low trapping level.

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CLAIMS

[Claim(s)]

[Claim 1] The manufacture approach of the semiconductor device characterized by making it the fluorine content of said semi-conductor layer become below 1.0x1019 (atoms/cm3) in manufacture of the semiconductor device with which a laminating is carried out and some constructs are formed on the 1 principal plane of a substrate so that the insulator layer and semi-conductor layer which consist of a silicon nitride may touch mutually.

[Claim 2] The manufacture approach of a semiconductor device according to claim 1 that an insulator layer and a semi-conductor layer are characterized by being continuously produced by the plasma chemistry gaseous-phase depositing method.

[Claim 3] The manufacture approach of a semiconductor device according to claim 1 that an insulator layer and a semi-conductor layer are characterized by being the gate dielectric film and the semi-conductor layer of a field effect transistor.

[Claim 4] The manufacture approach of a semiconductor device according to

claim 1 that a semi-conductor layer is characterized by being an amorphous silicone film.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the manufacture approach of a semiconductor device.

[0002]

[Description of the Prior Art] By the plasma chemistry gaseous-phase depositing method (it is henceforth called a plasma-CVD method), since it has the on resistance and off resistance which the thin film field-effect transistor (it is henceforth called a-Si TFT) respectively formed continuously as gate dielectric film and semi-conductor film excelled in the silicon nitride (it is henceforth called the SiNx film) and the amorphous silicone film (it is henceforth called the a-Si film), it is put in practical use as a switching element of a liquid crystal image display device.

[0003]

[Problem(s) to be Solved by the Invention] However, in those production processes, in case the interior of a process chamber of plasma-CVD equipment is cleaned using gas, such as NF3, CF4, and SF6, when a fluorine remains inside a process chamber and a fluorine mixes in the semi-conductor layer which formed membranes immediately after, there is a problem of degrading the on resistance of a-Si TFT and off resistance.
[0004] Then, this invention aims at offering the manufacture approach of semiconductor devices, such as a-SiTFT which improves the membraneous quality of a semi-conductor layer and has the outstanding dependability.
[0005]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, this invention is produced so that the fluorine content of the semi-conductor layer which removes the residual fluorine in a process chamber by the approach of generating the hydrogen plasma, and is produced by the plasma-CVD method after cleaning of the process chamber of plasma-CVD equipment may have a small value below 1.0x1019 (atoms/cm3).
[0006] By the improvement of the membraneous quality of a semi-conductor layer, this invention improves the membraneous quality near an interface, originates in that there are few trap levels, and can offer outstanding a-Si TFT of a property. Therefore, the thing of a property which was excellent also in the semiconductor device of other application using the semi-conductor layer of this invention is obtained.
[0007]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail with reference to a drawing. Drawing 1 shows the important section structure section of a-Si TFT in the gestalt of 1 operation of this invention. In drawing 1 , the gate electrode 2 which consists of conductors, such as Cr, aluminum, and Mo, is alternatively formed on a glass substrate 1.
[0008] After cleaning the interior of a process chamber of plasma-CVD equipment, the fluorine inside a process chamber is removed by generating the

hydrogen plasma.

[0009] By subsequently, the plasma-CVD method of an parallel monotonous mold for having used 13.56MHz glow discharge As gate dielectric film, the SiNx film 3 of the thickness of 3000x10-10m (or 3000A) extent, It deposits continuously. the a-Si film 5 of n+ mold which includes the a-Si film 4 of 2000x10-10m (or 2000A) extent, and Lynn as an impurity by the plasma-CVD method same as semi-conductor film as the SiNx film -- thickness 200x10-10m (or 200A) extent -- The a-Si film is alternatively removed by etching etc., and the pattern of the island-shape a-Si film is formed.

[0010] Furthermore, a-Si TFT is produced by forming the film which consists of conductors, such as Cr, aluminum, and Mo, on the pattern of the a-Si film 4 and the a-Si film 5 of n+ mold, and removing the n+ mold a-Si film between the source electrodes 6 and the drain electrodes 7 by which covering formation was alternatively carried out by etching etc.

[0011] On the property of a-Si TFT, and according to research of this invention persons, especially for an ON property and dependability, it is ******** to greatly be influenced by the membraneous quality of a semi-conductor layer. Especially, it was checked among the membraneous qualities of these semi-conductor layers that the amount of fluorine mixing is the big parameter which shows the optimal membraneous quality.

[0012] It is the same conditions as producing a-Si TFT, and the amount of fluorine mixing of the semi-conductor layer in the gestalt of this operation made the SiNx film and a semi-conductor layer deposit on the single crystal silicon substrate by which double-sided polishing was carried out, by secondary ion mass spectroscopy (SIMS), it carried out the quantum of the fluorine content per unit volume of a semi-conductor layer, and calculated it.

[0013] The shift of Vt of a same sign produces especially degradation of the a-Si TFT property by degradation of the membraneous quality of a semi-conductor layer by forward [of the sign of the gate voltage appeared and impressed to the threshold electrical potential difference Vt of the gate], and negative.

[0014] In a-Si TFT shown in drawing 1 , the threshold electrical potential difference Vt of the gate in the gestalt of this operation was made into gate voltage in case a drain current is set to 1x10-8A, when channel width W and the W/L ratio of the channel length L impressed uniformly a grounded source and drain electrical-potential-difference 0.1V in the environment of a dark place at the substrate temperature of 25.0**3.0 degrees C using the thing of 6. Moreover, Vt shift amount subtracts the gate threshold electrical potential difference Vt immediately after a-Si TFT production from the threshold electrical potential difference Vt when carrying out long duration actuation of a-Si TFT, and ending.
[0015] Drawing 3 shows the pattern of Vt shift of the fluorine content of a semi-conductor layer of a-Si TFT of 8.84x1019 (atoms/cm3). The property immediately after a-Si TFT production was A curve, and was Vt=Vt1**0.5V. The property after operating a-Si TFT in a 25.0**3.0-degree C environment among the desiccation nitrogen-gas-atmosphere mind of a dark place for 10 minutes by grounded source, grounded drain, and gate voltage 30V regularity (direct-current operating condition) is B curve. Vt=Vt2**4.5V, Vt showed the forward shift and the drain current in case gate voltage is 20V has decreased 11% with 2= 7.2micro [of ID] A in after what was initial ID1=8.1microA operating.
[0016] Drawing 2 changes various conditions of plasma CVD, such as a flow rate of hydrogen gas, discharge power, and a degree of vacuum, on the occasion of hydrogen plasma generating. About the semi-conductor layer produced after changing the amount of fluorines inside a process chamber, among the desiccation nitrogen-gas-atmosphere mind of a dark place, in a 25.0**3.0-degree C environment It is drawing which plotted Vt shift amount at the time of making it operate for 10 minutes by grounded source, grounded drain, and gate voltage 30V regularity (direct-current operating condition) on the axis of ordinate, and plotted the fluorine content of a semi-conductor layer on the axis of abscissa.
[0017] In drawing 2 , Vt shift amount of a-Si TFT is located in a line on two straight lines by making a fluorine content into a parameter. And when the fluorine content became larger than about 1.2x1019 (atoms/cm3), it became

clear that Vt shift amount increases with the increment in a fluorine content.
[0018] In order to obtain a-Si TFT excellent in dependability from the above thing, it turns out that it is required for the fluorine content of a semi-conductor layer to be small to below 1.0x1019 (atoms/cm3).
[0019]
[Effect of the Invention] As explained above, according to this invention, it is thought that the semi-conductor layer produced by the plasma-CVD method a fluorine content is small to below 1.0x1019 (atoms/cm3) has a small level consistency near an interface as mentioned above, and it excels as a semi-conductor layer of a semiconductor device. Furthermore, a-Si TFT using the semi-conductor layer of this invention has stable Vt shift, and can produce a-Si TFT which has the outstanding dependability.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The important section structure section Fig. of a-Si TFT in the gestalt of 1 operation of this invention
[Drawing 2] The property Fig. showing relation with Vt shift amount of a-Si TFT at

the time of performing direct-current actuation for 10 minutes with the fluorine content of a semi-conductor layer
[Drawing 3] The property Fig. in which having plotted the drain current on the axis of ordinate, having plotted gate voltage on the axis of abscissa, and having shown the situation of Vt shift
[Description of Notations]
1 Glass Substrate
2 Gate Electrode
3 SiNx Film
4 A-Si Film
5 N+ Mold A-Si Film
6 Source Electrode
7 Drain Electrode

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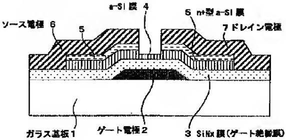
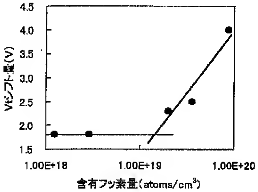
DRAWINGS

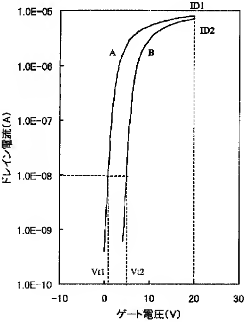
[Drawing 1]



[Drawing 2]



[Drawing 3]



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審査請求　未請求　請求項の数４　ＯＬ　（全４頁）

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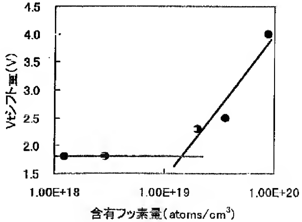
最終頁に続く

(54)【発明の名称】　半導体装置の製造方法

(57)【要約】
【課題】　プラズマＣＶＤ法でＳｉＮｘ膜とａ－Ｓｉ膜とがゲート絶縁膜及び半導体層として連続的に形成されてなるａ－Ｓｉ　ＴＦＴは優れたオン抵抗，オフ抵抗を有するが、製造過程において半導体層に混入するフッ素がオン抵抗，オフ抵抗を劣化させる原因となる。そこで、半導体層の膜質を改善し、優れた信頼性を有するａ－Ｓｉ　ＴＦＴの製造方法を提供する。
【解決手段】　プラズマＣＶＤ法で作製される半導体層のフッ素含有量を１．０×１０^19（atoms/cm^3）以下の小さな値を有するように作製する。この半導体層の膜質の改善により、ゲート絶縁膜との界面付近の膜質を良化し、トラップ準位が少ないことに起因して、Ｖｔシフト量の少ない優れた特性のａ－Ｓｉ　ＴＦＴを提供することができる。



【特許請求の範囲】

【請求項１】　基板の一主面上に、シリコン窒化膜からなる絶縁膜と半導体層とが互いに接するように積層されて一部の構成体が形成される半導体装置の製造において、前記半導体層のフッ素含有量が１．０×１０^{19}（atoms/cm^{3}）以下になるようにしたことを特徴とする半導体装置の製造方法。

【請求項２】　絶縁膜および半導体層が、プラズマ化学気相堆積法によって連続して作製されたことを特徴とする請求項１記載の半導体装置の製造方法。

【請求項３】　絶縁膜および半導体層が、電界効果型トランジスタのゲート絶縁膜と半導体層であることを特徴とする請求項１記載の半導体装置の製造方法。

【請求項４】　半導体層が、非晶質シリコン膜であることを特徴とする請求項１記載の半導体装置の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、半導体装置の製造方法に関するものである。

【０００２】

【従来の技術】プラズマ化学気相堆積法（以後、プラズマＣＶＤ法と呼ぶ）でシリコン窒化膜（以後、ＳｉＮｘ膜と呼ぶ）と非晶質シリコン膜（以後、ａ－Ｓｉ膜と呼ぶ）が各々、ゲート絶縁膜及び半導体膜として連続的に形成された薄膜電界効果トランジスタ（以後、ａ－Ｓｉ　ＴＦＴと呼ぶ）は優れたオン抵抗，オフ抵抗を有することから、液晶画像表示装置のスイッチング素子として実用化されている。

【０００３】

【発明が解決しようとする課題】しかし、それらの作製過程において、プラズマＣＶＤ装置のプロセスチャンバー内部をNF_3，CF_4，SF_6などのガスを用いてクリーニングする際に、プロセスチャンバー内部にフッ素が残留し、直後に成膜した半導体層にフッ素が混入することによって、ａ－Ｓｉ　ＴＦＴのオン抵抗，オフ抵抗を劣化させるという問題がある。

【０００４】そこで本発明は、半導体層の膜質を改善し、優れた信頼性を有するａ－ＳｉＴＦＴ等の半導体装置の製造方法を提供することを目的とするものである。

【０００５】

【課題を解決するための手段】上記目的を達成するため、本発明は、プラズマＣＶＤ装置のプロセスチャンバーのクリーニング後に、水素プラズマを発生させる等の方法でプロセスチャンバー内の残留フッ素を除去し、プラズマＣＶＤ法で作製される半導体層のフッ素含有量が１．０×１０^{19}（atoms/cm^{3}）以下の小さな値を有するように作製するものである。

【０００６】本発明は、半導体層の膜質の改善により、界面付近の膜質を良化し、トラップ準位が少ないことに起因して、優れた特性のａ－Ｓｉ　ＴＦＴを提供することができる。従って、本発明の半導体層を用いた他の応用の半導体装置も優れた特性のものが得られる。

【０００７】

【発明の実施の形態】以下、本発明の実施の形態について、図面を参照して詳細に説明する。図１は本発明の一実施の形態におけるａ－Ｓｉ　ＴＦＴの要部構造断面を示したものである。図１において、ガラス基板１上にＣｒ，Ａｌ，Ｍｏ等の導電体からなるゲート電極２を選択的に形成する。

【０００８】プラズマＣＶＤ装置のプロセスチャンバー内部をクリーニングした後に、水素プラズマを発生させることによりプロセスチャンバー内部のフッ素を除去する。

【０００９】次いで、１３．５６ＭＨｚのグロー放電を用いた平行平板型のプラズマＣＶＤ法で、ゲート絶縁膜として３０００×１０$^{-10}$m（又は３０００Å）程度の膜厚のＳｉＮｘ膜３と、半導体膜としてＳｉＮｘ膜と同じプラズマＣＶＤ法で２０００×１０$^{-10}$m（又は２０００Å）程度のａ－Ｓｉ膜４及びリンを不純物として含むｎ＋型のａ－Ｓｉ膜５を膜厚２００×１０$^{-10}$m（又は２００Å）程度連続的に堆積し、エッチング等でａ－Ｓｉ膜を選択的に除去して島状のａ－Ｓｉ膜のパターンを形成する。

【００１０】さらに、ａ－Ｓｉ膜４とｎ＋型のａ－Ｓｉ膜５のパターン上にＣｒ，Ａｌ，Ｍｏ等の導電体からなる膜を形成し、エッチング等で選択的に被着形成されたソース電極６とドレイン電極７との間のｎ＋型ａ－Ｓｉ膜を除去することにより、ａ－Ｓｉ　ＴＦＴが作製される。

【００１１】ａ－Ｓｉ　ＴＦＴの特性において、本発明者らの研究によると、特にオン特性と信頼性は、半導体層の膜質によって大いに左右されることが解かった。特に、これらの半導体層の膜質の内でフッ素混入量が最適な膜質を示す大きなパラメータであることが確認された。

【００１２】本実施の形態における半導体層のフッ素混入量は、ａ－Ｓｉ　ＴＦＴを作製するのと同じ条件で、両面研摩された単結晶シリコン基板上にＳｉＮｘ膜と半導体層とを堆積させ、二次イオン質量分析（ＳＩＭＳ）によって、半導体層の単位体積あたりのフッ素含有量を定量して求めた。

【００１３】半導体層の膜質の劣化によるａ－Ｓｉ　ＴＦＴ特性の劣化は、特にゲートのしきい値電圧Ｖｔに現れ、印加したゲート電圧の符号の正，負により同符号のＶｔのシフトが生じる。

【００１４】本実施の形態におけるゲートのしきい値電圧Ｖｔは、図１に示すａ－Ｓｉ　ＴＦＴにおいて、チャンネル幅Ｗ，チャンネル長ＬのＷ／Ｌ比が６のものを用い、基板温度２５．０±３．０℃で暗所の環境の中でソース接地，ドレイン電圧０．１Ｖを一定に印加した時に

ドレイン電流が１×１０$^{-8}$Ａになる時のゲート電圧とした。またＶｔシフト量はａ－Ｓｉ　ＴＦＴを長時間動作させ終了した時のしきい値電圧Ｖｔからａ－Ｓｉ　ＴＦＴ作製直後のゲートしきい値電圧Ｖｔを減じたものである。

【００１５】図3は、半導体層のフッ素含有量が８．８４×１０^{19}（atoms/cm^3）のａ－Ｓｉ　ＴＦＴのＶｔシフトの模様を示したものである。ａ－Ｓｉ　ＴＦＴ作製直後の特性がA曲線であり、Ｖｔ＝Ｖｔ１≒０．５Ｖであった。ａ－Ｓｉ　ＴＦＴを暗所の乾燥窒素ガス雰囲気中２５．０±３．０℃の環境でソース接地、ドレイン接地、ゲート電圧３０Ｖ一定（直流動作条件）で１０分動作させた後の特性がB曲線であり、Ｖｔ＝Ｖｔ２≒４．５Ｖと、Ｖｔが正のシフトを示し、ゲート電圧が２０Ｖの場合のドレイン電流は初期ＩＤ１＝８．１μＡであったものが動作後ではＩＤ２＝７．２μＡと１１％減少してしまっている。

【００１６】図2は、水素プラズマ発生に際し、水素ガスの流量，放電パワー，真空度等のプラズマＣＶＤの条件を種々変えて、プロセスチャンバー内部のフッ素量を変えた後に作製した半導体層について、暗所の乾燥窒素ガス雰囲気中２５．０±３．０℃の環境で、ソース接地，ドレイン接地，ゲート電圧３０Ｖ一定（直流動作条件）で１０分動作させた時のＶｔシフト量を縦軸に、半導体層のフッ素含有量を横軸にプロットした図である。

【００１７】図2において、フッ素含有量をパラメータにすることにより、ａ－Ｓｉ　ＴＦＴのＶｔシフト量が2つの直線上に並ぶ。そしてフッ素含有量が約１．２×１０^{19}（atoms/cm^3）より大きくなると、Ｖｔシフト量がフッ素含有量の増加とともに増大することが明らかになった。

【００１８】以上のことから、信頼性に優れたａ－Ｓｉ　ＴＦＴを得るには、半導体層のフッ素含有量が１．０×１０^{19}（atoms/cm^3）以下に小さいことが必要であることが解る。

【００１９】

【発明の効果】以上説明したように、本発明によれば、フッ素含有量が１．０×１０^{19}（atoms/cm^3）以下に小さいプラズマＣＶＤ法で作製された半導体層は、前述したように界面付近の準位密度が小さく、半導体装置の半導体層として優れていると考えられる。更に、本発明の半導体層を用いたａ－Ｓｉ　ＴＦＴはＶｔシフトが安定しており、優れた信頼性を有するａ－Ｓｉ　ＴＦＴを作製することができる。

【図面の簡単な説明】

【図１】本発明の一実施の形態におけるａ－Ｓｉ　ＴＦＴの要部構造断面図

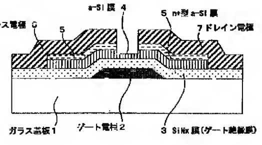
【図２】半導体層のフッ素含有量と直流動作を１０分間行った場合のａ－Ｓｉ　ＴＦＴのＶｔシフト量との関係を示す特性図

【図３】縦軸にドレイン電流、横軸にゲート電圧をプロットし、Ｖｔシフトの様子を示した特性図

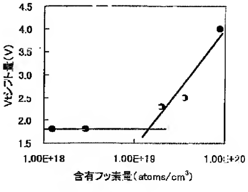
【符号の説明】

１　ガラス基板
２　ゲート電極
３　ＳｉＮｘ膜
４　ａ－Ｓｉ膜
５　ｎ＋型ａ－Ｓｉ膜
６　ソース電極
７　ドレイン電極

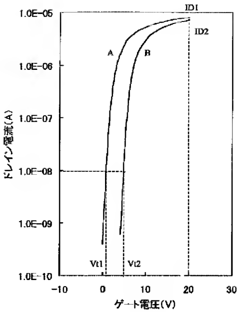
【図1】



【図2】



【図3】



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